PWM VLSI Neural Network for Fault Diagnosis[1)]

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Abstract An improved pulse width modulation (PWM) neural network VLSI circuit for fault diagnosis is presented, which differs from the software-based fault diagnosis approach and exploits the merits of neural network VLSI circuit. A simple synapse multiplier is introduced, which has high precision, large linear range and less switching noise effects. A voltage-mode sigmoid circuit with adjustable gain is introduced for realization of different neuron activation functions. A voltage-pulse conversion circuit required for PWM is also introduced, which has high conversion precision and linearity. These 3 circuits are used to design a PWM VLSI neural network circuit to solve noise fault diagnosis for a main bearing. It can classify the fault samples directly. After signal processing, feature extraction and neural network computation for the analog noise signals including fault information, each output capacitor voltage value of VLSI circuit can be obtained, which represents Euclid distance between the corresponding fault signal template and the diagnosing signal, The real-time online recognition of noise fault signal can also be realized.

Key words Pulse signal, fault diagnosis, neural network, noise, pulse width modulation, VLSI

1 Introduction

Differing from the traditional software-based and vibration-based approach for fault diagnosis, and exploitting the merits (high speed, parallel, *etc.*) of neural network VLSI circuit, a hardware-based and noise-based analog neural network VLSI pulse stream technique for mechanism fault diagnosis is presented.

In [1], the author presented an improved pulse width modulation (PWM) neural network VLSI circuit. A simple synapse multiplier was designed, which has high precision, large linear range and less switching noise effects. A voltage-mode sigmoid circuit with adjustable gain was designed for realization of different neuron activation functions. A voltage-pulse conversion circuit required for PWM was also suggested, which has high conversion precision and linearity. In [2], a design idea of fault diagnosis system based on PFM (pulse frequency modulation) was proposed.

This paper describes the PWM VLSI neural network circuit consisting of the three circuits in [1,3] to diagnose gap abrasion fault of a main bearing. After signal processing, feature extraction and neural network computation for the analog noise signals including the fault information, each output capacitor voltage value of the PWM VLSI circuit, which represents Euclid distance between the corresponding fault signal template and the diagnosing signal, can be obtained, then the fault can be recognized.

Firstly, a new FET (field effect transistor) synapse multiplier/adder based on analog pulse stream is used to realize the operation of neural network. Moreover, because of adopting the algorithm of shortest-distance classifier based on single-level perceptron network, the synapse weight values need not to learn. Certainly, for some complex fault diagnosis including a lot of mechanical equipment and fault types, multi-level neural network (BP, Kohonen) should be used. Secondly, fault diagnosis and condition monitoring on most parts of diesel (including piston, valve, *etc.*) are often based on vibration signals because vibration sensor is easy to approach those parts and sensitive to their abrasion. However, a main bearing locates in the interior of diesel, it would result in a lot of troubles of disassembling a diesel engine to install vibration sensors near the main bearing.

As in [2], noise measurement of diesel is used to realize the monitoring and fault diagnosis of the gap abrasion of the main bearing. The operation of the reciprocating diesel is a non-stationary shock vibration, and its energy has a wide distribution in the frequency domain. From the ordinary

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spectrum, it is very difficult to find fault signatures like those of rotating machinery. In our software-based approach of fault analysis, the extraction of fault signature based on noise signal and wavelet envelope spectrum was applied to the condition monitoring of gap abrasion of the main bearing, as in [2], and the result showed that it was very simple and effective and could make the best use of the conditions information.

2 Experiment conditions

In order to realize the hardware-based online monitoring of the gap abrasion conditions of the main bearing, the testing equipment is specially set up as shown in Fig. 1. This testing engine is connected with a waterpower loadometer with adjustable output power. A ND_2 acoustic detector is used to sample the noise signals of the diesel. The capacitor microphone of acoustic detector should be located on the same horizontal level with the main bearing of diesel, so its distance to the diesel is 0.8m, and its height to the ground is 0.75m. The noise of diesel is usually emitted up and down along the vibration direction, and relatively stronger in some directions and weaker in other directions. So the first step is to scan the surface of diesel for a best measurement position where the radiation effect of sound energy is best, as in [2].

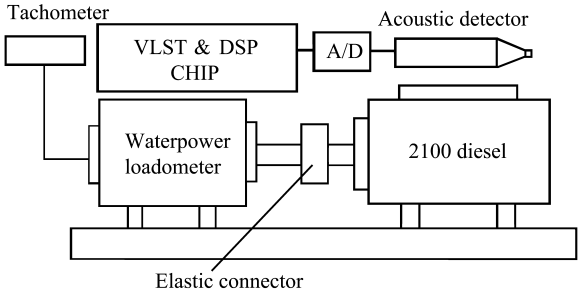

Fig. 1 Sketch map of testing equipment

In order to obtain measurement results exactly, it is necessary to simulate five conditions of gap abrasion of the main bearing (0.12mm, 0.20mm, 0.22mm, 0.26mm, 0.30mm). The limit value of gap abrasion of the testing main bearing is 0.25mm, so the above five testing gap conditions include basically all work conditions from normal gap to serious gap abrasion. In addition, rotating speed: $1200r/\text{min}$, output power: 80%, sample rate: 10.8KHz, sample length: 8192 points.

The noise signals of the diesel can be transformed into time-frequency domain through orthogonal wavelet. Appropriate frequency band is selected and its envelope spectrum is made by Hilbert transform. Through signal analysis, it is found that the amplitude values of $0.5\times$ rotating speed frequency, $1.5\times$ rotating speed frequency, $2\times$ rotating speed frequency and cepstrum 100ms are very sensitive to the gap abrasion conditions of the main bearing, as in [2]. Finally, the four signature values are imported into the analog neural network circuit through D/A and PWM encoding. In addition, a DSP unit (Digital Signal Processor) is used to process signal analysis, and compute the above four signature values (including wavelet analysis, cepstrum analysis, *etc.*). Through D/A, the analog voltage forms of the above four signature values are imported into VLSI pulse stream circuit to perform condition recognition. In Fig. 1, all hardware units (A/D, D/A, DSP, PFM and VLSI neural network circuit) locate in a VLSI and DSP CHIP unit.

3 Designs for pwm neural net unit circuit

As in [1], artificial neural network (ANN) has many wide applications in pattern recognition, fault diagnosis, image processing, *etc.*, however, lacking of effective hardware circuit is still obstructive to its farther development. [3] proposed a digital-analogue merged pulse stream circuit that controls the operation of multiplier by digital signal, and has the merit of small area multiplier as well as anti-jamming capability of digital signal that represents the neuron state. But this approach would have more switching noise effects on the section of analogue circuit. Among many present approaches of pulse

modulation, PWM has come to many researchers' attention due to its facile circuit realization, as in [3∼7]. [3] also proposed another triple-tube multiplier that has simple structure and can realize PWM VLSI ANN synapse circuit; nevertheless it still has low precision, small linear range and low linearity. [4] used a simple structure, low gain double-tube amplifier to realize the nonlinear transform, but its transform function still has a large difference with ideal sigmoid function. Based on the above problems, [1,7,8] designed a simple synapse multiplier which has a high precision and large linear range, and a voltage-mode sigmoid circuit with adjustable gain according to a standard CMOS process, respectively. In addition, a voltage-pulse conversion circuit required for PWM was also suggested as below.

3.1 Single-level perceptron neural network

In this experiment, it only includes five types of fault conditions, so the simplest decision-making unit based on single-level perceptron (input vector, synapse weights, perceptrons/output vector) is used. It can obtain the Euclid distance between standard fault and input testing vector through hardware-based neural network operation, and then can classify each input pattern. The form of single-level perceptron is as below.

$$V_K = f_h(\sum_j T_{kj} V_j) \tag{1}$$

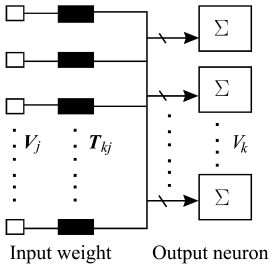

Fig. 2 Single level perceptron network

where $\boldsymbol{V}_j$ is the j^{th} element of input vector; V_K is the k^{th} element of output perceptrons/output vector; T_{kj} is the synapse weight value between $\boldsymbol{V}_j$ and V_K; f_h is a non-linear function.

Each synapse weight vector is initialized directly by corresponding standard fault signature vector. The output perceptron V_K represents one fault type, and the input vector $\boldsymbol{V}_j$ represents one testing vector to be diagnosed. Through the operation of neural network, each V_K can give an output value representing the Euclid distance value between the current input testing vector $\boldsymbol{V}_j$ and the corresponding synapse weight vector $\boldsymbol{T}_{kj}$. Through finding the minimum Euclid distance value, the class of current fault can be obtained. (Certainly, for complex and large-scale fault recognition, multi-level BP neural network should be recommended)

3.2 Synapse multiplier

The basic principle of PWM synapse multiplier is: the analogue signal that represents input neuron state is modulated as pulse signal, and the pulse width is proportional to the analogue signal; Then, the pulse controls an electric current for the integral of a capacitor, the voltage of which is proportional to the product of input state signal and weight value. The scheme of the PWM synapse multiplier is shown as Fig. 3. The left frame is the synapse multiplier unit, and the right one is the integral-adding unit. For the aim of simplification, Fig. 3 only draws one unit of the synapse multiplier. Actually, there are many output electric currents of synapse multiplier units to finish the adding function through the same integral adding unit. In Fig. 3, transistor M_1 and M_2 consist of a voltage-electric current transform circuit. Suppose V_{TP} and V_{TN} are the threshold voltage of M_1 and M_2, respectively, k_1 and k_2 are the conductance factors of M_1 and M_2, respectively; if $V_{REF} + V_{TP} \leqslant V_W \leqslant V_{REF} + V_{TN}, k_1 = k_2, V_{TN} = -V_{TP}, V_{CC} = 2V_{REF}$, then I_B, the difference of electric current between M_1 and M_2, is linear with $V_W - 1/2V_{CC}$

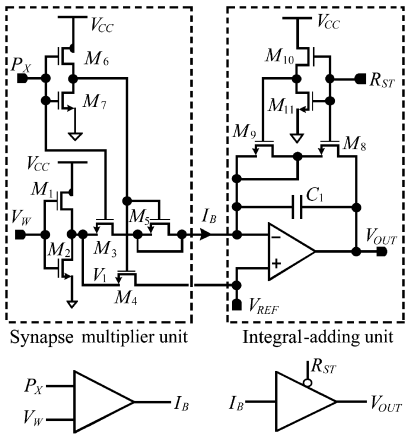

Fig. 3 PWM synapse multiplier circuit

$$I_B = -2k_1(V_{CC} - 2V_{TN})(V_W - \frac{1}{2}V_{CC}) \tag{2}$$

P_X, the pulse signal representing input neuron state, controls the on/off state of integral electric current I_B through switch transistor M_3. The function of M_4 is to make V_1 equal to V_{REF} so as to ensure the steady work conditions of M_1 and M_2 when M_3 is on or off, and improve the output precision. The work process of synapse multiplier unit is as follows firstly. Pulse signal R_{ST} makes the output integral voltage V_{OUT} reset to V_{REF} through the on-control of M_8; then, electric current I_B starts to charge capacitor C_1, and the charge time length is equal to the pulse width (T_{WIDTH}) of P_X. Consequently, the final result is as below.

$$V_{out} - \frac{1}{2}V_{CC} = \frac{1}{C_1}\int_0^{T_{WIDTH}} -I_B \mathrm{d}t = \frac{2k_1 T_{WIDTH}}{C_1}(V_{CC} - 2V_{TN})(V_w - \frac{1}{2}V_{CC}) \tag{3}$$

Namely, the variation of V_{OUT} is linear with the multiplicative value of $(V_W - 1/2V_{CC})$ and T_{WIDTH}, and thereby finishing the multiplicative operation of neural network indirectly. In order to minish the disturbance effect from P_X and R_{ST}, two extra MOS transistors (M_5, M_9) are placed into the above circuit, and the width/length ratio of $M_5(M_9)$ is just 1/2 of that of $M_3(M_8)$. The above circuit design can eliminate the switching noise effect on the operational amplifier.

3.3 Sigmoid transform circuit

The implementation includes the electric current-model and voltage-model, as in [1,7,8]. There are different requirements for sigmoid function gain in different applications, so a voltage-mode sigmoid circuit with adjustable gain is designed for realization of different neuron activation functions. In Fig. 4, V_{IN} is input voltage, V_{REF} is reference voltage, V_{CTRL} is control voltage to adjust gain, and V_{OUT} is output voltage.

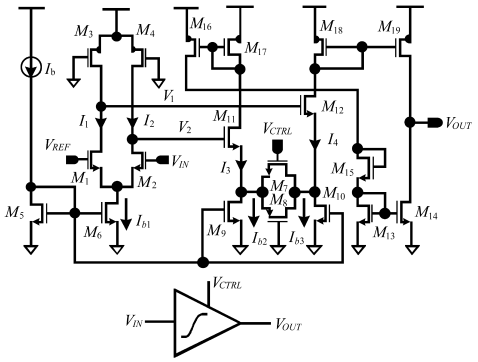

Fig. 4 Voltage-mode sigmoid circuit with adjustable gain

M_1 and M_2 controlled by V_{REF} and V_{IN} comprise an input differential-couple operating under saturation condition, and the difference of electric currents between M_1 and M_2 is as below.

$$I_1 - I_2 = \frac{1}{2} = \frac{1}{2}\beta_1(V_{REF} - V_{IN})\sqrt{\frac{4I_{b1}}{\beta} - (V_{REF} - V_{IN})^2} \tag{4}$$

In (4), β_1 is a constant, M_3 and M_4 are the resistances of M_1 and M_2, respectively. If resistance value is R_M, then the voltage difference between two input ports of the second-stage input differential-couple is as below.

$$V_2 - V_1 = (I_1 - I_2)R_M = \frac{1}{2}\beta_1 R_M(V_{REF} - V_{IN})\sqrt{\frac{4I_{b1}}{\beta_1} - (V_{REF} - V_{IN})^2} \tag{5}$$

M_8 is an ever-through resistance. The resistance value of M_7 is controlled by V_{CTRL}, which adjusts the intensity of feedback of differential-couple to change the gain of circuit. If under the extreme condition that the resistance values of M_7 and M_8 are all zero, then the difference of electric currents between M_{11} and M_{12} under the saturation condition is as below.

$$I_3 - I_4 = \frac{1}{2}\beta_2(V_2 - V_1)\sqrt{\frac{4(I_{b2} + I_{b3})}{\beta_2} - (V_2 - V_1)^2} \tag{6}$$

In (6), β_2 is a constant, if $|V_{REF} - V_{IN} << \min\left\{\sqrt{\frac{4I_{b1}}{\beta_1}}, \frac{2}{R_M}\sqrt{\frac{I_{b2} + I_{b3}}{I_{b1}\beta_1\beta_2}}\right\}$, then

$$I_3 - I_4 = \frac{1}{3}\beta_1\beta_2 R_M(V_{REF} - V_{IN})\sqrt{\frac{4I_{b1}}{\beta_1} - (V_{REF} - V_{IN})^2}\sqrt{\frac{I_{b2} + I_{b3}}{\beta_2}} \tag{7}$$

V_{OUT}, the output voltage activized when electric currents (I_3 and I_4) pass through a series of current-mirrors, can be defined approximately as below.

$$V_{OUT} = 2.5 + K(I_3 - I_4) \tag{8}$$

In (8), K is a constant, so the final form of VOUT can be denoted as

$$V_{OUT} = 2.5 + \frac{1}{2}k\beta_1\beta_2 R_M(V_{REF} - V_{IN})\sqrt{\frac{4I_{b1}}{\beta_1} - (V_{REF} - V_{IN})^2}\sqrt{\frac{I_{b2} + I_{b3}}{\beta_2}} \tag{9}$$

And it can approximate to a sigmoid function:

$$V_{OUT} = \frac{5}{1 + e^{-C(V_{IN} - 2.5)}} \quad C \text{ is a constant} \tag{10}$$

3.4 Voltage-pulse conversion circuit

Comparing with those conventional digital-based or analogue-based neural network circuits, the pulsed signals can simplify the operation circuits (*e.g.*, synapse circuit) and improve the inter-linkage density among neurons effectively. The pulsed signals can also simplify the interfaces between neural network chips and other peripherals (*e.g.*, computers, digital circuit, *etc*). Due to the good anti-jamming performance, it can make the communications inside one neural network chip and among neural network chips more reliable. However, as concerning a large-scale fault recognition, because of the limited recognition ability of a single neural network chip, multi chips need to run parallel with each other. Just as it is, pulse stream technique can represent its superiority of supporting the communication among chips, as in [3].

Because of the pulse transmission form of neuron state information, the input voltage signals and the output voltage signals of sigmoid activation function transform should be transformed into pulse signals. In Fig. 5, a voltage-pulse conversion circuit required for PWM is presented, which has high conversion precision and linearity. V_V is input voltage, V_P is output pulse signal, C_{TRL} is control signal. When C_{TRL} is at high level, M_5 is on, and M_6 is off, as a result, the voltage (V_1) of capacitor C_1 keeps 0 V, and V_P is at low level. When CTRL is from high level to low level, and $V_1 < V_V$, the output of the comparator composed of $M_{11} \sim M_{15}$ is reversed, and V_P is from low level to high level. And then, because M_5 is off and M_6 is on, I_B begins to charge the capacitor C_1 with constant current, accordingly, V_1 also begins to increase linearly form 0 V. Once V_1 exceeds V_V, the output of the comparator is reversed again, and V_P changes into low level. Consequently, the pulse width of V_P (output signal) can be defined as below.

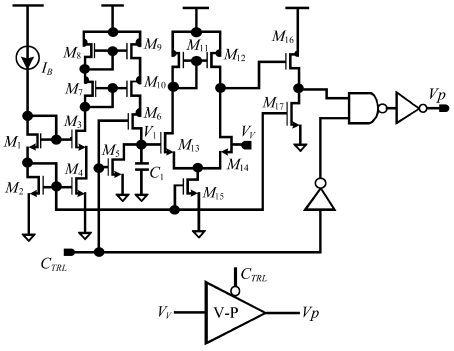

Fig. 5 Voltage-pulse conversion circuit

$$T_{WIDTH} = C_1\frac{V_V}{I_B} \tag{11}$$

Namely, the pulse width of output signal is just linear with the input voltage.

4 Noise recognition test based on PWM VLSI neural networks

In our simulation test, single-level perceptron network is used to implement fault recognition. There are five faults of gap abrasion, and each can be diagnosed through 4 signature parameters as shown in Section 2. Therefore, the chip should include 5 neurons and 20 synapses. This method includes two aspects. The first is to extract fault signature vectors from noise signals instead of vibration signals, and the second is to use pulse stream (PWM), FET synapse multiplier and single-level perceptron network to implement fault recognition.

The input data of VLSI chip is a 4-dimensional (4-D) signature vector. A model for recognizing five conditions of gap abrasion of 2100-diesel (0.12mm, 0.20mm, 0.22mm, 0.26mm, 0.30mm, from normal

gap to serious abrasion) is designed. Each standard fault template vector U_K (K=1∼5) represents four amplitude values of 0.5×speed frequency, 1.5×speed frequency, 2×speed frequency and cepstrum 100ms,and directly stored in the memory of the chip. The sampled noise signal is imported into VLSI circuit through amplifier and A/D. DSP processor makes a five-level symlets 4 wavelet decomposition for each group of 8192 points of noise signal, and extracts its envelope of high frequency band; finally, it performs a spectrum analysis of the envelope and obtains the above four signature values. Each 4-D signature template vector of 8192 points is saved in memory consecutively. Consequently, the sequences of all standard fault template vectors of the five conditions of gap abrasion can be obtained. If the length of noise signal is W points, then $W/8192$ template vectors U_K will be saved for each fault condition. In this simulation test, the W is 81920. In our previous software based research, as in [2], it is proved that all the above four signature values increase along with the increment of gap abrasion.

In fact, the chip includes a shortest-distance classifier based on pulse stream and neural network to obtain the Euclid distance between the input testing vector and each fault template vector. In this test, there are 5 perceptrons on a chip, so it can classify 5 fault types. However, if two chips are used to recognize faults, then each standard fault template can have two versions for a higher precision. In order to obtain the highest precision, it is also necessary to mark the noise signal sample. The angle range is from -360° to 360° during a work cycle of the diesel. During the course of experiment, record each maximum pressure value while breaking off oils and regard it as 0°. Through the above steps, it can be assured that the length of noise signal is integral multiple of a work cycle of the diesel. In addition, the work condition of extracting fault templates should be consistent with that of recognizing faults in the future.

During the process of real-time fault recognition, DSP will output a new 4-D vector $\boldsymbol{x}$ to be diagnosed after A/D samples a group of 8192 points, then the four signature values of vector $\boldsymbol{x}$ also need to be transformed into analog voltage form, and encoded using PWM to produce the input state vector $\boldsymbol{v}_j$. Correspondingly, every 4-D fault template vector $\boldsymbol{u}_k$ stored in memory is read sequentially, and transformed into analog voltage through D/A. Therefore, as soon as finishing the transform from $\boldsymbol{x}$ to $\boldsymbol{v}_j$, the analog voltage form of each vector $\boldsymbol{u}_k$ is imported into the corresponding position, as synapse weight vector T_{kj} of this frame (one frame is 8192 points). In our test, $W = 81920$, so the system needs to loop the above steps for 10 frames to compute the Euclid distance values between $\boldsymbol{x}$ and 5 $\boldsymbol{u}_k$ vectors respectively ($\boldsymbol{k} = 1 \sim 5$, five fault conditions).

$$\| \boldsymbol{x} - \boldsymbol{u}_k \|^2 = \| \boldsymbol{x} \|^2 - 2\boldsymbol{u}_k^{\mathrm{T}}\boldsymbol{x} + \| \boldsymbol{u}_k \|^2 \tag{12}$$

The first item of the above equation is the same to all '$\boldsymbol{k}$', so it can be neglected. Then, the equation is as below:

$$G_K(\boldsymbol{x}) = -2(\boldsymbol{u}_k^{\mathrm{T}} - \frac{1}{2}\boldsymbol{u}_k^2) = -2(\boldsymbol{w}_k^{\mathrm{T}}\boldsymbol{x} + W_{k_0}) \tag{13}$$

In (13), $G_K(\boldsymbol{x})$ is a linear function, $\boldsymbol{w}_k = \boldsymbol{u}_k, \boldsymbol{w}_{k_0} = -1/2\boldsymbol{u}_k^2$.

If set $\boldsymbol{w}_k = \{T_{kj}\}$ which is the synapse weight vector, and $\boldsymbol{x} = \{V_j\}$, then

$$g(G_K(\boldsymbol{x}) = \sum_{j=1}^{j=4} T_{kj}V_j + W_{k_0} \tag{14}$$

gG_K can compute the distance between $\boldsymbol{x}$ and each $\boldsymbol{u}_k$, This can just realize the shortest-distance classifier. Due to the negative symbol of (13), the K^{th} $\boldsymbol{u}_k$, which makes gG_K in (14) have the greatest output, is just nearest to $\boldsymbol{x}$. During the period of each frame, according to equation (14), all Euclid distance values between $\boldsymbol{x}$ and five fault templates are computed, and the results in five output capacitors (output neurons) on VLSI chip are stored. In fact, storing the results through capacitors means that the results from sequential frames can be accumulated. Finally, "the most active" output neuron having the highest output voltage after sampling 81920 points is found. Each corresponding fault type that each output neuron represents has been marked in advance, so fault which happened can be recognized right away now.

In our simulation test, a threshold value must be also defined. If $D_m (m = 1 \sim 5)$ are the five Euclid distance values, and $D_{\min} = \min\{D_m\}$, then the difference between the five D_m values and

$D_{\min}$ is: $C_m = |D_m - D_{\min}|$. In terms of testing experience, the threshold value (V_d) is defined as 0.2. If there is only one $C_m < V_d$, then the fault is just the type that the m-th output neuron represents; otherwise, if there are more than one $C_m < V_d$, then the fault reason can not be judged.

Table 1 is part of the simulation results (using level 47 transistor models for a standard 1.2 μ_m CMOS process). In Table 1, $D_1 \sim D_5$ are the Euclid distance values between one testing vector $\boldsymbol{x}$ and five standard fault template vectors $\boldsymbol{u}_k$; $\boldsymbol{s}_1 \sim \boldsymbol{s}_4$ are 4 testing vectors $\boldsymbol{x}$; R represents the recognition results, and Gap1∼Gap5 represent the diagnostic results of gap conditions.

Table 1 Euclid distance between standard fault templates and testing samples

	D_1	D_2	D_3	D_4	D_5	R
$\boldsymbol{s}_1$	−1.17	−0.69	1.05	2.11	3.98	Gap1
$\boldsymbol{s}_2$	−1.53	−2.60	−1.67	0.09	1.31	Gap2
$\boldsymbol{s}_3$	−1.31	−2.58	−4.21	−3.93	−2.12	Gap3
$\boldsymbol{s}_4$	0.79	−2.71	−3.01	−4.11	−2.85	Gap4
$\boldsymbol{s}_5$	1.27	−3.22	−4.01	−4.17	−4.58	Gap5

In our 25 testing samples ($\boldsymbol{s}_1 \sim \boldsymbol{s}_{25}$), there were only 2 samples that could not be recognised after the validation of threshold value. So the precision of recognition can reach 80% or so.

5 Conclusions

Comparing with other circuits based on analog, digital or analog/digital, the neural network VLSI circuit using pulse stream technique can lessen the complexity of VLSI and noise disturbance, increase the density of neurons and make chip communicate with other digital circuits or PCs more easily. Through this simulation, it is proved that its performance is near to that of the software-based fault diagnosis system. In addition, for some complex and large-scale fault monitoring, the multi-level perceptrons BP neural network VLSI circuit and its dynamic learning of weight values should be considered, as in [3∼6], because it has a better performance than the shortest-distance classifier based on single-level perceptron network, even though the shortest-distance classifier does not need to train synapse weight values.

For other aspects of VLSI pulse stream technique, such as switch capacitor circuit, dynamic storing of weight values and improvement of anti-jamming performance of circuit, please refer to other relevant books.

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