

Energy-aware System Design for Wireless Sensor Network¹⁾

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Abstract Wireless sensor networks have already enabled numerous embedded wireless applications such as military, environmental monitoring, intelligent building, *etc.* Because micro-sensor nodes are supposed to operate for months or even years with very limited battery power source, it is a challenge for researchers to obtain long operating hour without scarifying original system performances. In this paper, the energy consumption sources of the wireless sensor networks are firstly analyzed, with the digital processing and radio transceiver units being emphasized. Then, we introduce the design scheme of our energy-aware wireless sensor network (GAINS). In GAINS, techniques to conserve the energy are exploited including the energy optimization node, software and energy-efficient communication protocol. The design architecture of our ultra low power wireless sensor network (WO-LPP) is specially presented.

Key words Wireless sensor network, GAINS, DVS, MAC

1 Introduction

Recently interest has been drawn into building and deploying wireless sensor networks. Wireless sensor networks are autonomous *ad hoc* networks designed for some potential applications in environmental monitoring, surveillance, military, health, security and so on. Distributed micro-sensor network consists of many small, extensible nodes. A sensor node is made up of four basic components as shown in Fig. 1: a sensing unit, a processing unit, a transceiver unit and a power unit. Once the nodes are deployed into the target area, they collect data from the environment automatically and establish *ad hoc* networks to transfer their data to base stations. The base stations aggregate and analyze the reported messages and decide whether there is an unusual or concerned event occurrence in the deployed area^[1,2].

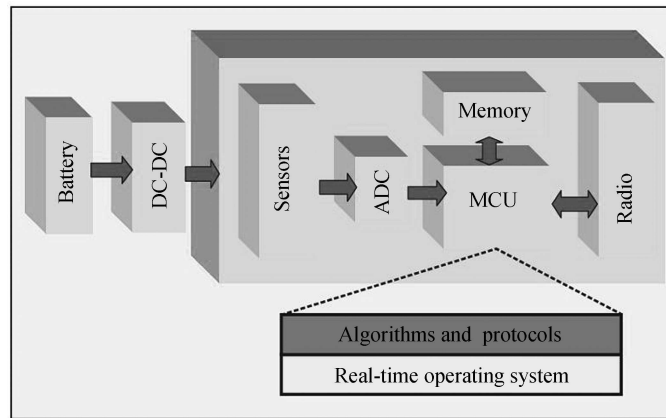


Fig. 1 Components of sensor node

For wireless sensor networks, energy source provided for sensor nodes is usually battery power. The sensor nodes must have lifetime of months or years, since it is undesirable even impossible to recharge or replace the battery power of the thousands of sensor nodes^[3,4]. Therefore, energy efficiency has become the crucial design challenge in sensor networks. Conventional low power design techniques emphasize on the energy consumption in circuit and architecture level of the single node^[5]. However,

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maximizing the system life of the whole network is our purpose. The system life is measured by the time span before all nodes have been drained out of their battery power or the network no longer provides an acceptable event detection ratio, which directly affects network usefulness. Therefore, energy awareness must be integrated into every stage of wireless sensor network design to maximize the system life.

The rest of the paper is organized as follows. Section 2 analyzes the energy consumption sources in wireless sensor network including sensing unit, digital processing unit, and radio transceiver unit. In Section 3, we design an energy-aware network by using the following energy-conserving techniques: 1) energy optimization in node circuit, 2) energy-aware software for sensor network. The architecture of the proposed ultra low power design for wireless sensor network (WO-LPP) is detailed in the paper and other novel energy-aware techniques used in our system are presented as well.

2 Energy consumption in wireless sensor network

Before the discussion of energy-aware wireless sensor network design, the energy consumption characteristics of a sensor node is analyzed in three parts: the sensing circuitry, the digital processing unit, and the radio transceiver.

2.1 Sensing unit

The sensing unit, which is composed of environmental sensors and A/D converter, translates physical phenomena to electrical signals. There are several sources of energy consumption in sensor unit: 1) signal sampling and conversion of physical signals to electrical ones, 2) signal conditioning, 3) analog-to-digital conversion. The energy consumption in this unit is relatively constant, and improvements to their energy efficiency depend on increasing integration and skilled analog circuit design. And it also has been tested that passive sensors such as temperature, seismic, *etc.*, consume negligible energy compared to other components in sensor nodes. So, in the following section, we will emphasize on the energy consumption of the digital processing unit and radio transceiver unit^[4].

2.2 Digital processing unit

The majority of digital circuits employed in wireless sensor network nodes are typically used in command and control functions, baseband signal processing unit and implementation of the protocol stack. The energy consumed in a digital circuit is determined by the sum of dynamic and static power dissipation^[6~8].

$$P_d = P_{dyn} + P_{stat} \quad (1)$$

The dynamic power is described as CV_{DD}^2 , with C representing the switched capacitance and V_{DD} the gate supply voltage. Static dissipation originates from the undesirable leakage of current from power to ground at all times and is described by $I_0e^{V_{DD}/nV_{TH}}$, where V_{TH} is the threshold voltage of the transistors, I_0 and n are constants for the process technology.

$$P_d = CV_{DD}^2 + (t + V_{DD})I_0e^{V_{DD}/nV_{TH}} \quad (2)$$

In the hardware of a wireless sensor network, the number of gates undergoing a transition cycle at any one time can be very small, on average, due to the very low duty cycles supported by their communication protocol. So the leakage power dominates the total power. Since the leakage power is proportional to time, slowing down the clock will actually increase the amount of leakage power. The easiest way to reduce leakage power is to shut down the power supply to idle components, which is called power gating. But it is noted that shutting down complicated circuits can cause time and energy overhead. The methods to solve those problems and conserve energy in digital circuit will be introduced in Section 3.

2.3 Radio transceiver unit

Wireless communication is the major energy consumer during system operation. It is difficult to generalize energy consumption by communication system, as many variables influence the performance. Generally, the energy consumption of the radio consists of two components: 1) an RF component that depends on the transmission distance and modulation parameters; 2) an electronics component that accounts for the energy consumed by the circuitry that performs frequency synthesis, filtering, up-converting, *etc.* The energy required for a complete radio transmission can be described as follows^[8].

$$P_{tx}(T_{transmit} + T_{start}) + (P_{out}T_{on}) \quad (3)$$

where P_{tx} represents the power of the transmitter electronics, $T_{transmit}$ the transmit duration, T_{start} the startup time, and $P_{out}T_{on}$ the radiated energy. The startup time T_{start} is our specific concern. The

packets transmitted by the radio are likely to be small during idle periods because of the low data rates of the sensor network. The startup power will dominate the power of active transmission. While the radio's high bias currents require acceptance of shutdown cost, the node should amortize the startup power over more transmitted bits to reduce the power cost per bit of transmissions.

Besides the factor pointed above, there are other reasons leading to the energy dissipation in radios. Generally, radios can operate in four distinct modes of operation: transmit, receive, idle and sleep. An important influencing factor is that a significant amount of energy is dissipated as the radio's operating mode changes. As shown in Table 1, most radios operating in Idle mode result in significantly high energy consumption, almost equal to the energy consumed in the Receive mode.

Table 1 Radio power characterizations^[10]

Radio mode	Power consumption (MW)
Transmit	14.88
Receive	12.50
Idle	12.36
Sleep	0.016

Obviously, it is important to completely shut down the radio rather than switch it to idle mode when not transmitting or receiving data.

3 Energy-aware system design for wireless sensor network

In the above section, we explored the energy dissipations in wireless sensor nodes. To minimize the energy consumption, many techniques have been developed. In this section, we will introduce the design of our energy-aware system for wireless sensor network (GAINS). The techniques used in GAINS can be classified into the followings: 1) energy optimization in node circuit, 2) energy-aware system and 3) energy efficient communication protocol.

3.1 Energy optimization in sensor node circuit

The architecture of the ultra low-power processor (WO-LPP) used in GAINS nodes is introduced in this subsection. Some novel energy-aware techniques such as dynamic voltage scaling, Modulation scaling are also introduced which will be exploited in our GAINS nodes. Ultra low-power processor for wireless sensor network advances low-power circuit and system design has resulted in the development of ultra low power processor for sensor network^[9,10]. In fact, there are many low-power states for RF module and other peripheral device. The optimized low power processor design will contribute to efficient power controlling of the whole system as it is the headquarters of the system. Instead of minimizing the energy usage of conventional microprocessor, we have designed a low power processor WO-LPP especially for sensor nodes^[11].

Harvard architecture (separate memories and buses for program and data) is used in our low power processor to maximize performance and parallelism. Almost all the instructions in the program memory are executed with a simple three level pipelining. While one instruction is being executed, the next instruction is being pre-fetched from the in-system reprogrammable flash memory. Our processor has 8-bit RISC ISA CPU core with 4k SRAM, 64K on-chip program flash. Some peripheral devices, such as time counter, real time counter, ADC, SPI, I2C and UART communication interface are also integrated into the chip. The fast-access register file contains 32 x 8-bit general purpose working registers and 96x8-bit I/O status and control registers with a single clock cycle access time. This allows single-cycle arithmetic logic unit (ALU) operation. In a typical ALU operation, two operands are output from the register file, the operation is executed, and the result is stored back into the register file, all in one clock cycle.

A very significant innovation of our processor is that an on-chip power management unit (PMU) is built. The PMU which works under a relatively low frequency clock manages the event-based system tasks, and computes the resource and power. To our knowledge, the power management scheme which will be discussed later is firstly proposed in this paper. Better efficiency and performance can be achieved by this scheme.

Event-driven management mechanism

The most innovative work of our WO-LPP processor is the efficient scheme of combining system task, computing resource and power management scheme. As shown in Fig. 2, the intelligent power management policies are built into the PMU according to the system task runtime states and computing resource usage.

PMU is responsible for determination of sleep modes of all components automatically. At the same time, user can also control the mode through specific SLEEP instruction.

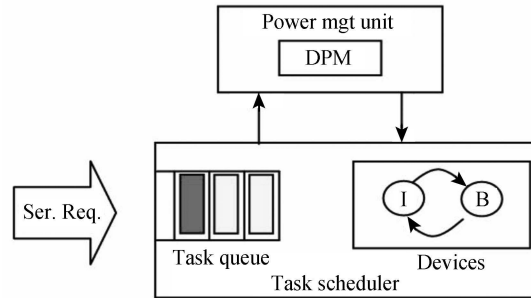


Fig. 2 System architect of WO-LPP

An intelligent hardware task scheduler is implemented to combine the task queue, PMU and other devices, which is not simply a FIFO, but an arbiter of all types of tasks with different priorities. There are two types of tasks in our system: system task (generated by internal interruption) and user-defined task (defined by software). A two-level priority tree which denotes the hierarchical organization of all tasks is used to guide the task scheduler. The system tasks induced by internal hardware interruptions have the highest priorities and then the sensing and communicating events; the last is low priority software transactions. The task priority information and the hardware resource usage information configured by compiler or users are directly marked in Task Queue when the task is posted.

WO-LPP begins by executing its boot code. The last instruction in the boot code is the special DONE instruction, which tells the instruction fetch unit to stop fetching instructions and to wait for an event token to appear at the head of the task queue. Event token indicates which occurred event can be inserted into the task queue by the task scheduler. If an event token is present at the head of the task queue, the instruction fetch unit will remove it and use it as an index into WO-LPP event-handler table to determine the address of the appropriate event handler. WO-LPP will execute the instructions starting at that address until it reaches another DONE instruction, at that time it will check the event queue again. If the event queue is empty when the DONE instruction is executed, WO-LPP will go to deep low power sleep mode. At the same time, when a task is scheduled, the hardware usage information is also passed into PMU, which can be used to decide whether to power down each function unit or not. Accurate power evaluation tools show the scheme can reduce system power consumption efficiently.

RISC-based instruction set

The system architecture and low power mechanism of our processor described above require several extensions to conventional RISC instruction sets. Our WO-LPP ISA contains instructions that can be classified into four categories:

- 1) Standard RISC instructions. Typical instructions are implemented in our processor, including arithmetic and logic instructions, jump and conditional branch instructions, and memory, general and I/O register-access instructions etc. The internal program bus is 16-bit and the data bus is 8-bit, which is enough for most of wireless sensor network applications. The five different addressing modes for the data memory are: direct, indirect with displacement, indirect, indirect with pre-decrement, and indirect with post-increment. In the 32×8-bit register file, registers R26 to R31 feature the indirect addressing pointer registers.

- 2) Peripheral communication instructions. WO-LPP has built in SPI, I2C, UART interface and a wireless radio frequency communication module, which will satisfy different applications. Five specific instructions performing the action commonly used in network code are implemented in WO-LPP ISA for simplicity. These instructions synchronize the processor core with peripheral devices through relevant configurable status and control registers.

- 3) Task schedule instructions. Our processor also has three extra instructions: POST, DONE and SLEEP to control the event-driven execution of the processor for software entrance of task and power management. POST is a 32-bit instruction, which can be used to generate a new task handler with priority and compute resource parameters transferred simultaneously. The programmer can also use the DONE instruction to indicate the end of a handler. When the instruction fetcher receives a

DONE instruction, it sends feedback to the task scheduler telling it to look for another token at the head of the event queue. Programmer can also use SLEEP instruction to realize software level power management. There are six different low power modes: Idle, Power-down, Power-save, Standby, and Extended Standby.

We have implemented the WO-LPP addressed above and realized a prototyping wireless sensor network node with it. The first generation wireless sensor network nodes (GAINS) based on WO-LPP are shown in Fig. 3. GAINS' nodes have been successfully used in wireless sensor network applications such as environment and security monitoring, *etc.*

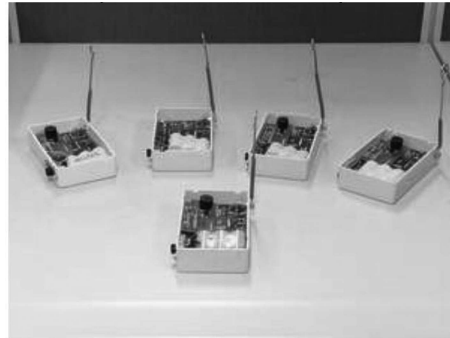


Fig. 3 WO-LPP based sensor nodes

Dynamic voltage & modulation scaling

While shutdown techniques can save energy by turning off idle components, additional energy savings are possible by optimizing the sensor node performance in the active state. Dynamic voltage scaling (DVS) is such a technique that can make intelligent trade-offs between energy and quality^[12]. Most microprocessor systems are characterized by time-varying computational load. Significant energy benefits can be achieved by realizing the peak performance being not always required. So reducing the supply voltage in conjunction with the clock frequency achieves energy savings for the actual computation. DVS exploits this fact by dynamically adapting the processor's supply voltage and operating frequency to meet the fluctuations of processor's utilization, thus trading off unutilized performance for energy savings. Dynamic voltage scaling capabilities have been demonstrated on the SA-1100, the processor chosen for the uAMPS wireless micro-sensor prototype.

Fig. 4 gives the energy consumption of the SA-1100 processing core versus the latency of computation (inverse of clock frequency) and the supply voltage. A DC-DC converter circuit with a digitally adjustable voltage delivers power to the SA-1100 core and is controlled by a multithreaded energy-aware operating system which will be introduced next. The SA-1100 operates at supply voltage of 1.5 Volts

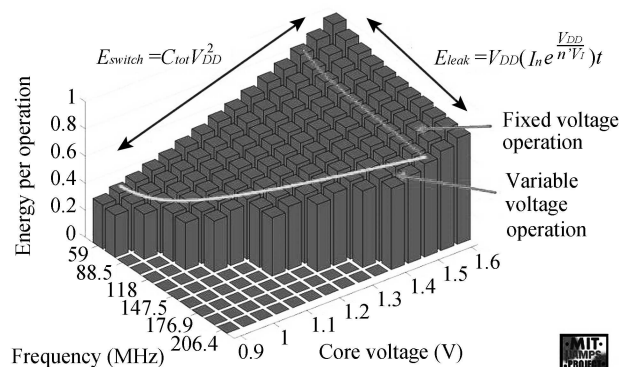


Fig. 4 Energy consumption per operation for the processor^[15]

and clock frequency in the range of 59MHz to 206MHz. We are designing a PCB containing a custom DC-DC converter circuit which provides a dynamically adjustable voltage to our WO-LPP. Those tech-

niques should be controlled by a multithreaded energy-aware operating system which will be discussed next.

At the circuit level, modulation scaling is a new technique, which exhibits benefits similar to dynamic voltage scaling in reducing sensor node's energy^[13]. It allows us to exhibit trade off energy against transmission delay and fidelity in communication. The communication energy per bit is a function of packet size and the modulation level (bits/symbol). When peak-workload is needed, the modulation level should be adapted higher for fast transmission to save energy. When the workload is low, transmissions can be slowed down. In Section 2, we have pointed out that the startup energy will dominate the energy of active transmission. Therefore, fast start-up low power transmitter is necessary for an energy efficient transmission. In future, we will design attractive transmitter architecture that meets these goals based on a fractional-N frequency synthesizer with modulator for our GAINS nodes. Higher loop bandwidth and faster start-up time can be achieved by those techniques.

3.2 Energy-aware software for wireless sensor network

To maximize the lifetime of the sensor node after its deployment, all aspects, including the software, should be energy efficient. Therefore, embedded operating systems, compiler and application software are critical in such wireless sensor networks. The design scheme is shown in Fig. 5, which has four levels: hardware, compiler, operating system and application software. The lowest level is processing, communicating and sensing hardware with compiler, assembler and emulator built above. The OS level is the most complicated level, which provides all API functions of the whole system resources. Here we only focus on some considerations of the OS and compiler.

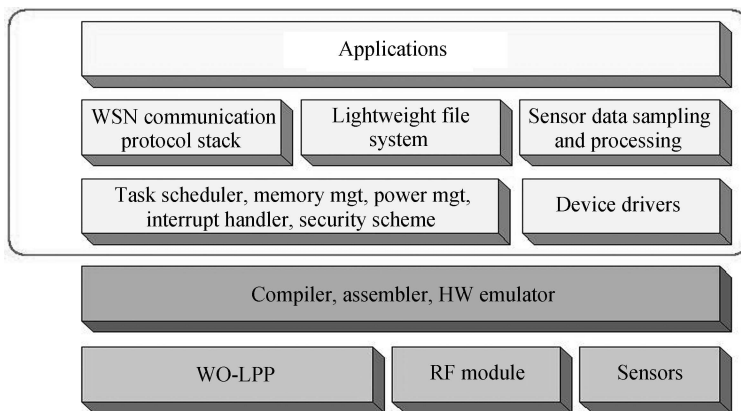


Fig. 5 Software frame of our sensor nodes

Traditional operating systems are not suitable for the wireless sensor network because of their inefficiency. TinyOS is an event-driven operating system especially for wireless sensor network designed by UC Berkeley. The characteristics of event-driven asynchronous naturally support the interactions and communications between modules of vastly different behavior and processing speeds in system, and the simplicity reduces overhead. The core of TinyOS is a task scheduler, which is responsible for scheduling a given set of tasks to run on the system while ensuring that timing constraints are satisfied. Scheduling algorithms provide the way to save energy by trading off energy against fidelity and predicting the computation requirements of individual task instances.

Since the operating system has the globe view of the system, it is ideally to implement the shut-down-based and DVS-based power management policies. Dynamic power management (DPM) is an OS-directed power management technique to improve the energy efficiency of sensor nodes^[12]. The basic idea is to shut down devices when not needed and to wake them up when necessary. But sleep-state transitioning has the overhead (storing processor state and turning off power) and wake up also takes up time. Fig. 6 shows five different sleep states for the sensor node. Each of these node sleep modes corresponds to an increasingly deeper sleep state and is therefore characterized by an increasingly deeper sleep state and decreasing power consumption^[12].

Our wireless sensor network operating system composed of many components is much fatter than application software. Some specific functions are directly moved to OS level for higher level, such as

power manager, sensor data processor and communication protocol stack, security scheme, *etc.* Light weighted file system, device drivers, task scheduler (mainly realized in WO-LPP) and memory manager have become very slim to achieve very high real-time property (the response time is important for sensor network). Efficient event-based power management is an important component, which is integrated with task scheduler and communication protocol. Dynamic power management has also been implemented in our OS, which is responsible for the states transition and management.

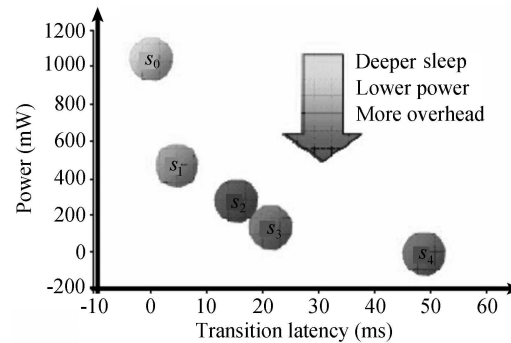


Fig. 6 Different states of the sensor node^[15]

Because C language which is commonly used in most applications provides the low-level features necessary for accessing hardware and the convenience for programming, it is used to produce efficient program code for our WO-LPP. Popular C compiler GCC is enhanced for WO-LPP to shorten the development cycle. But the wireless sensor network application software composed of many different components is very different from one to another. In fact, one application has only a few hardware components. So it is necessary for wireless sensor network software to have an overall function call analysis to delete the unused function units from the whole system during compiling. This is so-called overall call analysis compiler.

3.3 Energy-efficient communication protocol

The network-level schemes and protocols should also be energy aware for the energy efficient network. The protocol stack used by the sensor nodes consists of the application layer, transport layer, network layer, data link layer and physical layer^[2]. Transport layer is especially needed when the system is planned to be accessed through Internet or other external networks, it is not quite associated with the goal of saving energy. Physical layer solutions related to energy aware have also been introduced in Section 2. Therefore, the energy management in wireless sensor network will be emphasized in network layer and data link layer.

Medium access control (MAC) layer is responsible for the multiplexing of data streams, data frame detection, medium access and error control. Many MAC layer protocols have been studied since the layer gives a fine-grained control to switch the wireless radio on and off. The fundamental question MAC layer energy save mechanism answers is: When should a device switch to a low power mode and for how long. The MAC protocol used in our GAINS network is S-MAC. S-MAC is a protocol developed specifically to address energy issues in sensor networks. It uses a simple scheduling scheme to allow neighbor to sleep for long periods and synchronize wakeups. In S-MAC, nodes enter sleep mode when a neighbor is transmitting and fragment long packets to avoid costly retransmissions. It is designed to save energy on single radio architecture. Energy efficiency is always an important consideration in network layer protocols of wireless sensor network. Energy-aware routing protocol ensures the survivability of low energy networks. The protocols do not find a single optimal path to use for communication. They keep a set of good paths and choose one using probability. This means that instead of a single path, communication uses different paths at different times, thus any single path does not deplete energy. The Directed Diffusion protocol has been tested in the testbed of our GAINS. The effect of the protocol has been proved to be more energy efficient compared to the single multi-hop protocol.

4 Conclusion and future work

Wireless sensor networks are emerging as a solution for a wide range of data gathering applications. The most substantial challenge before designers is how to reduce the energy consumption to maximize

the lifetime of the whole network. In this paper, we have firstly analyzed all kinds of factors of energy dissipation. An energy-aware system (GAINS) for wireless sensor network using current energy efficient techniques are introduced. An ultra low-power processor for wireless sensor network (WO-LPP) used in GAINS is presented in detail. Other novel techniques such as DVS and modulation scale are also included. Based on the GAINS nodes, we have also developed our operating system, compiler and protocol stack. Our future work will highlight the survivability life of the whole network. Therefore, the application algorithms integrated with other layer's protocol will be the focus of our future research.

References

- 1 Kahn J, Katz R, Pister K. Next century challenges: Mobile networking for smart dust. In: Proceedings of ACM International Conference on Mobile Computing and Networking (MOBICOM'99). Washington: ACM Press, 1999. 271~278
- 2 Akyildiz I F, Su W, Sankasubramaniam Y, Cayirci E. Wireless sensor networks: A survey. *Computer Networks*, 2002, **38**(4): 393~422
- 3 Chandrakasan A P, Amirtharajah R, Cho S H, Goodman J, Konduri G, Kulik J, Rabiner W, Wang A. Design considerations for distributed microsensor systems. In: Proceedings of Custom Integrated Circuits Conference, San Diego, California: IEEE Press, 1999. 263~270
- 4 Raghunathan V, Schurgers C, Park S, Srivastava M B. Energy-aware wireless microsensor networks. *IEEE Signal Processing Magazine*, 2002, **19**(2): 40~50
- 5 Wentzloff D D, Calhoun B H, Min R, Wang A, Ickes N, Chandrakasan A P. Design considerations for next generation wireless power-aware microsensor nodes. In: Proceedings of the 17th International Conference on VLSI Design (VLSID'04). 2004. 361~367
- 6 Doherty I, Warneke B A, Boser B E, Pister K S J. Energy and performance considerations for smart dust. *International Journal of Parallel and Distributed Systems and Networks*, 2001, **4**(3): 121~133
- 7 Hac A. *Wireless Sensor Network Designs*. The Atrium, Southern Gate, Chichester, West Sussex PO19 8SQ, England: John Wiley & Sons Ltd, 2003
- 8 Furht B. *Wireless Sensor Networks Architectures and Protocols*. New York, USA: John Wiley & Sons Inc, 2004
- 9 Kelly C, Ekanayake V N, Manohar R. SNAP: A sensor-network asynchronous processor. In: Proceedings of the 9th IEEE Symposium on Asynchronous Circuits and Systems, Vancouver, BC, Canada: IEEE Press, 2003. 132~140
- 10 Ekanayake V, Kelly C, Manohar R. An ultra low-power processor for sensor networks. *ACM Signal Notices*, 2004, **39**(11): 27~36
- 11 Xu Y J, Liu L Y, Shen P F, Lv T, Li X W. Low power processor design for wireless sensor network applications. In: Proceedings of International Conference on Wireless Communications, Networking, and Mobile Computing (WCNM 2005), Wuhan China: IEEE Press, 2005. 883~886
- 12 Sinhua A, Chandrakasan A. Dynamic power management in wireless sensor network. *IEEE Design and Test of Computer*, 2001, **18**(2): 62~74
- 13 Wang A, Cho S H, Sodini C G, Chandrakasan A P. Energy-efficient modulation and MAC for asymmetric microsensor systems. In: Proceedings of International Symposium on Low Power Electronic Devices and Design, California: IEEE Press, 2001. 106~111

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